HACKING A 1991 VINTAGE XILINX 2K/3K DEMO BOARD

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&
Squeaky Hinge
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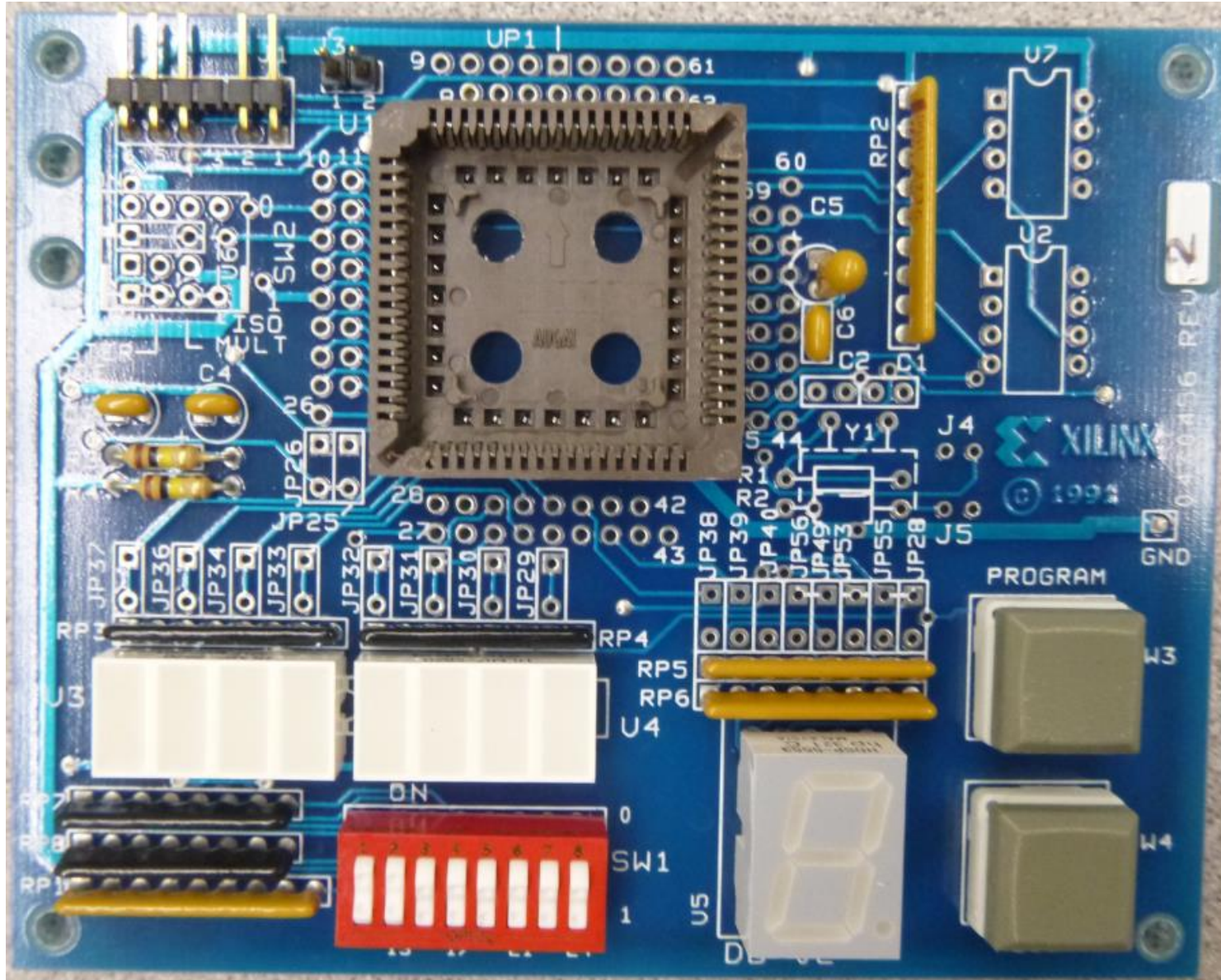
XC2000/XC3000 DEMO BOARD

- This board is essentially a set of resources that can be used with and Arduino or Raspberry Pi. In it's former life it was a Xilinx XC2064 or XC3020 Field Programmable Gate Array (FPGA) demo board... It was Awesome... but that was 1991
  - Eight individual LEDS
  - One 7SEG display
  - Eight DIP switches
  - Two Pushbutton Switches

XC2000/XC3000 DEMO BOARD

SUPER... AWESOME... XC3020A

Device	XC3020A XC3020L XC3120A	XC3030A XC3030L XC3130A	XC3042A XC3042L XC3142A XC3142L	XC3064A XC3064L XC3164A	XC3090A XC3090L XC3190A XC3190L	XC3195A
Gates	1,000 to 1,500	1,500 to 2,000	2,000 to 3,000	3,500 to 4,500	5,000 to 6,000	6,500 to 7,500
CLBs	64	100	144	224	320	484
Row x Col	(8 x 8)	(10 x 10)	(12 x 12)	(16 x 14)	(20 x 16)	(22 x 22)
IOBs	64	80	96	120	144	176
Flip-flops	256	360	480	688	928	1,320
Horizontal Longlines	16	20	24	32	40	44
TBUFs/Horizontal LL	9	11	13	15	17	23
Bits per Frame (including1 start and 3 stop bits)	75	92	108	140	172	188
Frames	197	241	285	329	373	505
Program Data = Bits x Frames + 4 bits (excludes header)	14,779	22,176	30,784	46,064	64,160	94,944
PROM size (bits) = Program Data + 40-bit Header	14,819	22,216	30,824	46,104	64,200	94,984

Figure 21:   Internal Configuration Data Structure for an FPGA. This shows the preamble, length count and data frames generated by the Development System.

XC3020 CLB
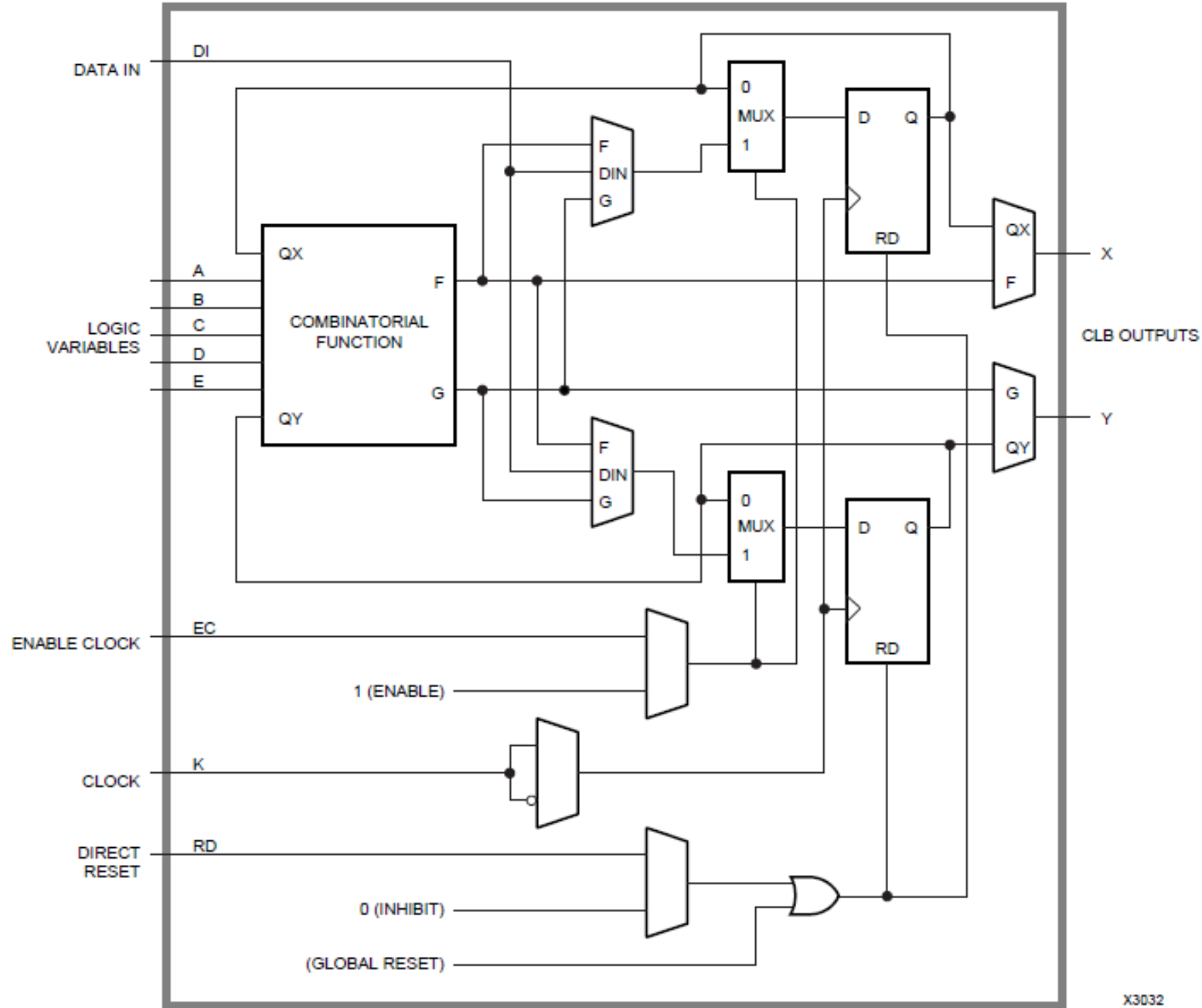
X3032

ROUTING, PIPS, CLBS

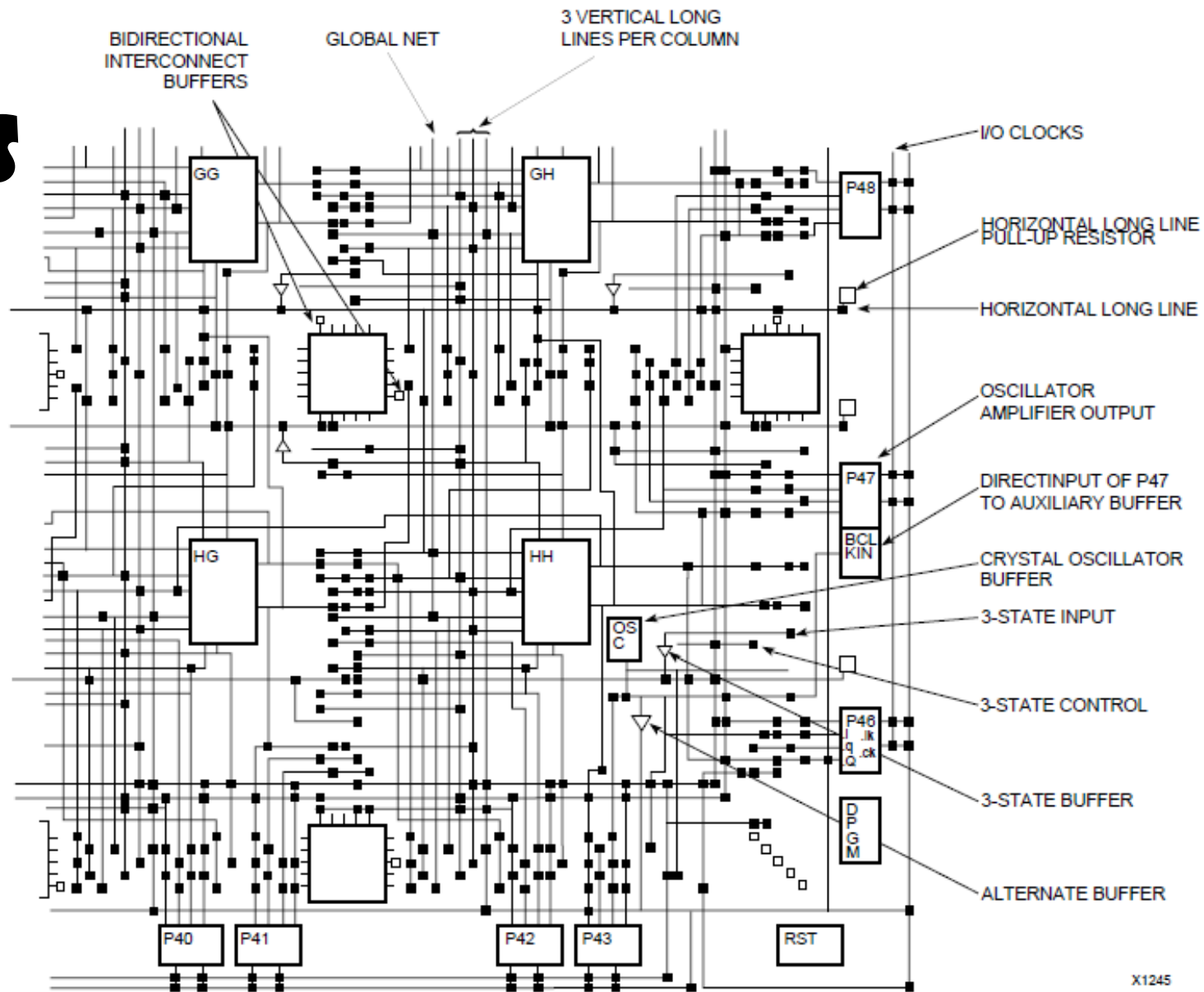**Figure 18: Design Editor.**
An extra large view of possible interconnections in the lower right corner of the XC3020A.

WHAT'S IT GOOD FOR?
POORMAN'S SHIELD OR PI HAT

- There are lots of examples of old development kits that have passed their usefulness, but still have resources that can be used to leverage with a Arduino or Raspberry Pi

- Typically you can remove the original chip and still access the LED's and Switches

- Is my program working?
  - Arduino's at least have one built in LED
  - Raspberry Pi's don't have any useful built in LED that can be used to indicate a program I/O
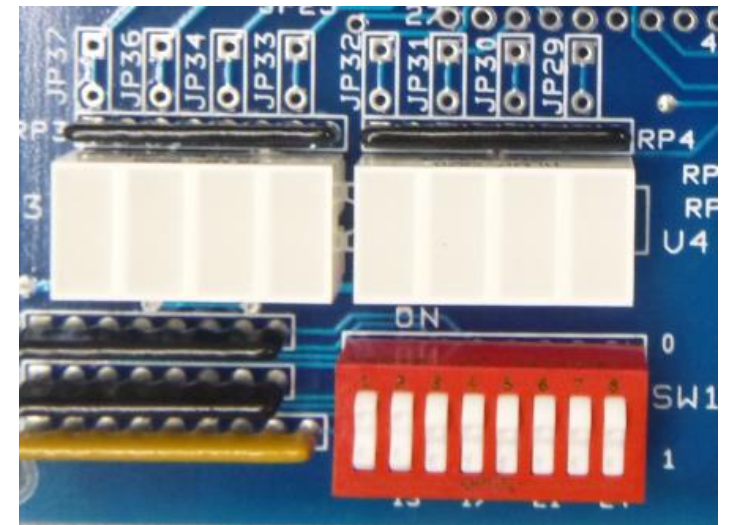
LAB TIME – QUESTION TIME

- What was the main feature of this board? Why was it build?
- What are the 4 types of General Purpose Input/Output (GPIO)?
- How many GPIO pins are needed for the LED?
- What about the 7Segment Display?
- What are the small yellow/orange strips next to the LEDs, 7Seg, Switches?
- Why are they there?

XILINX DEMO BOARD

- Main Reason was to show off and demo the Xilinx XC3020A device
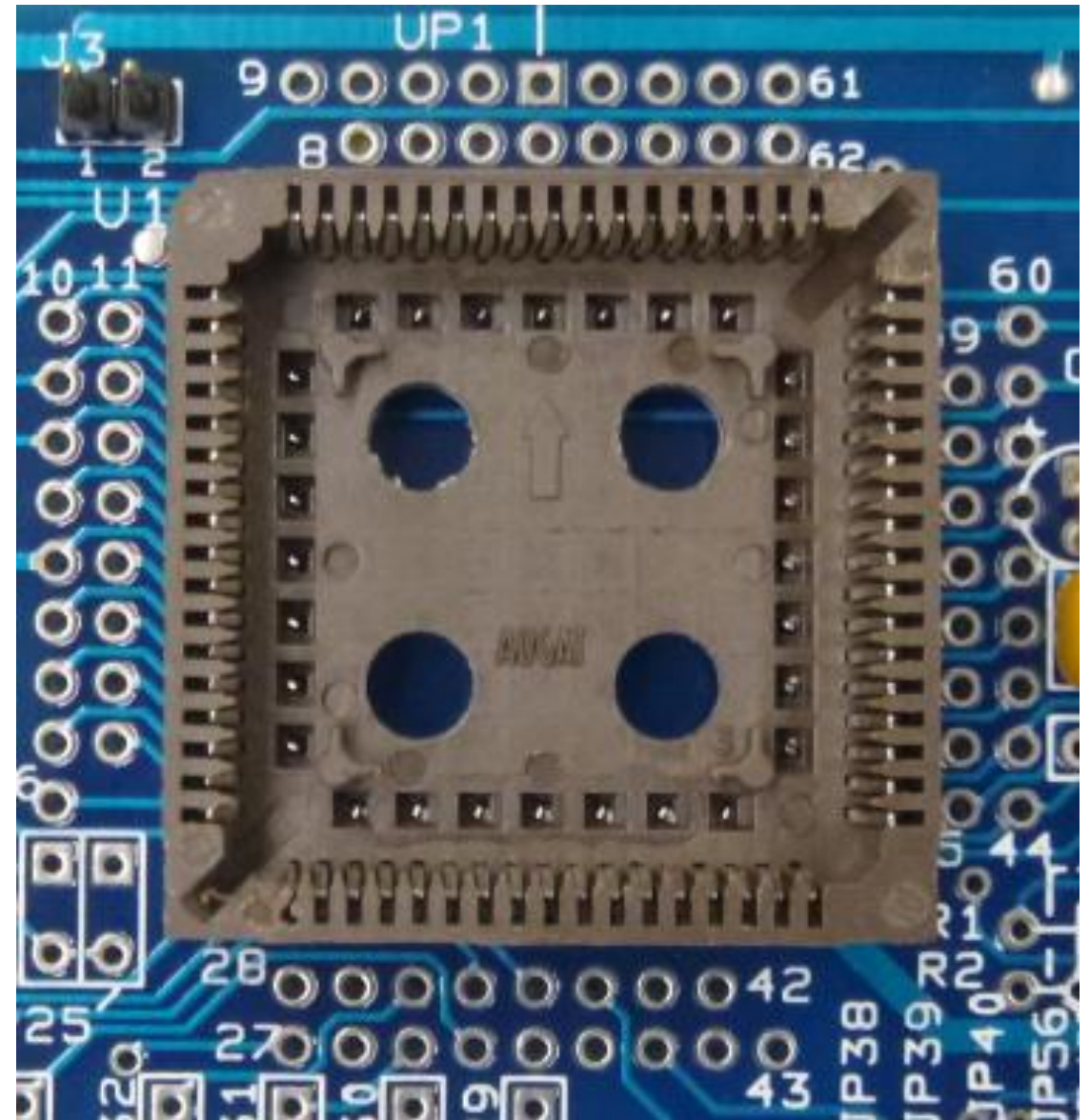
HOW MANY GPIO PINS ARE NEEDED FOR LEDS?
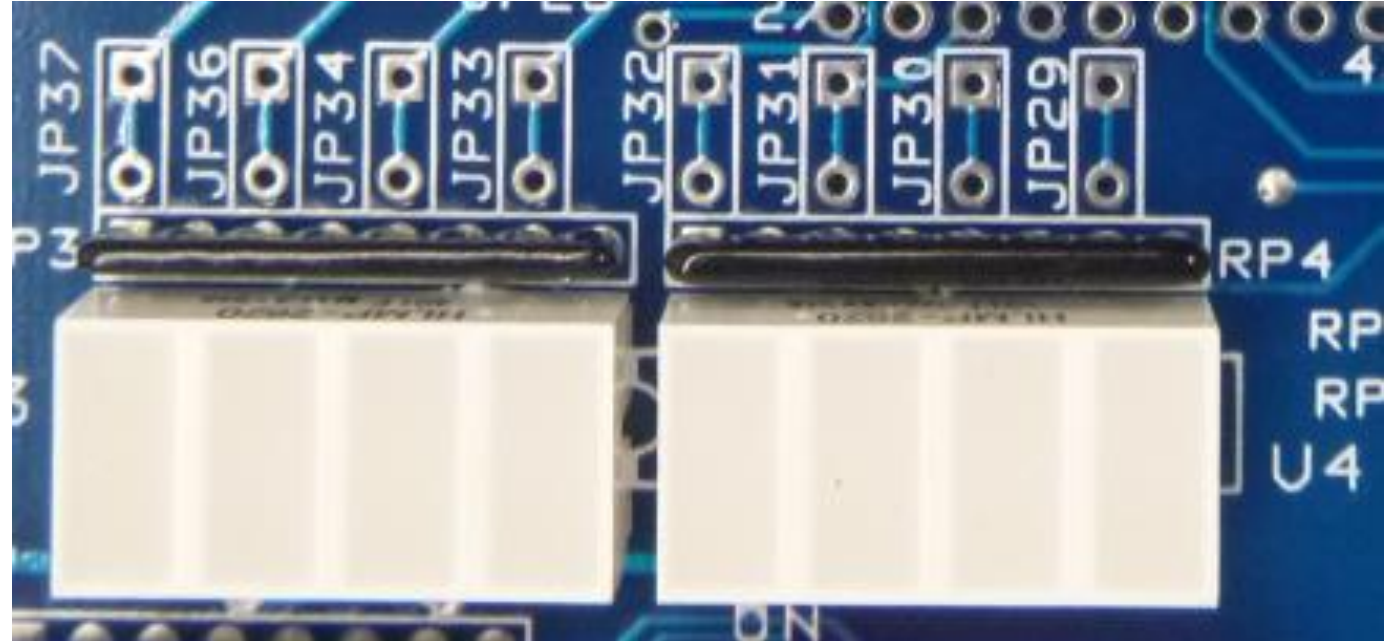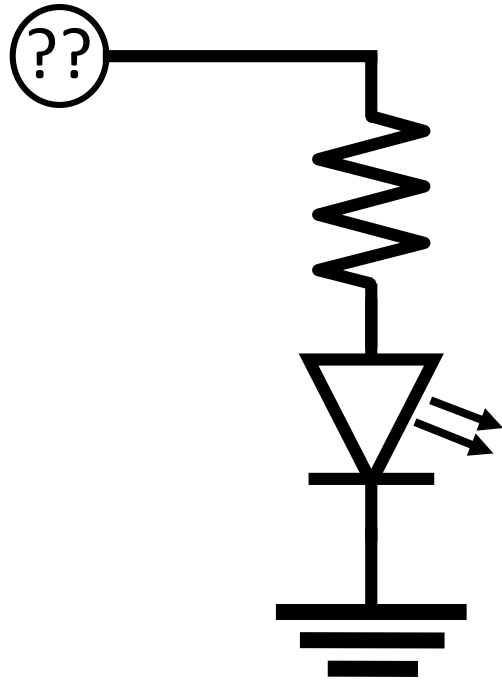
WHAT ABOUT GPIO FOR THE 7SEGMENT DISPLAY?

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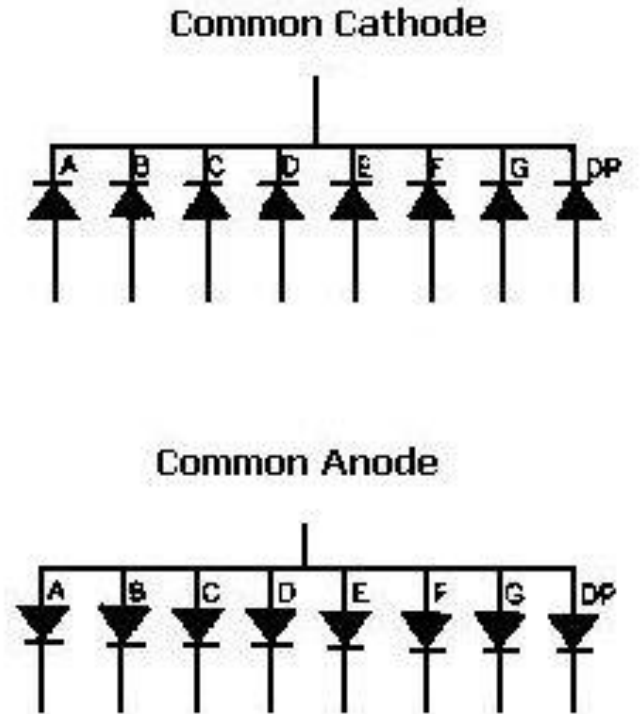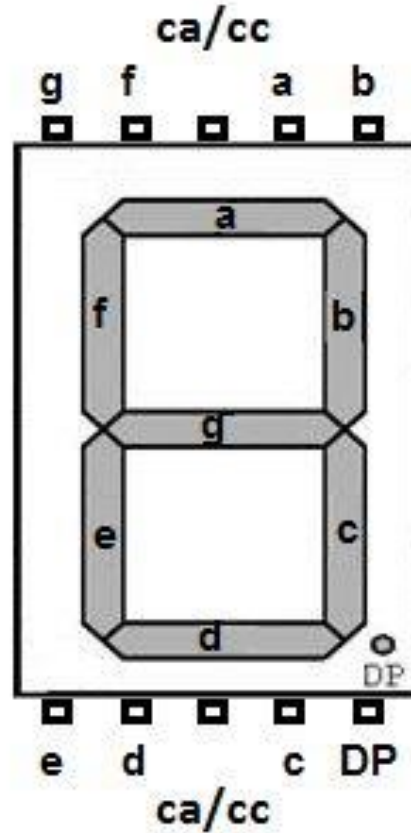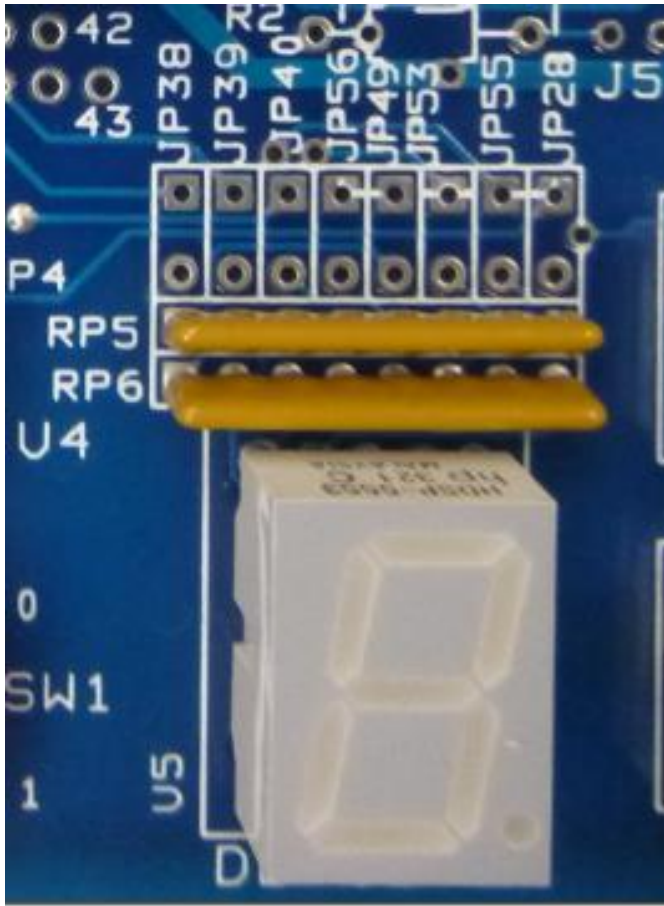
WHAT ARE THESE?

- What are the small yellow/orange strips next to the LEDs, 7Seg, Switches?
- Why are they there?
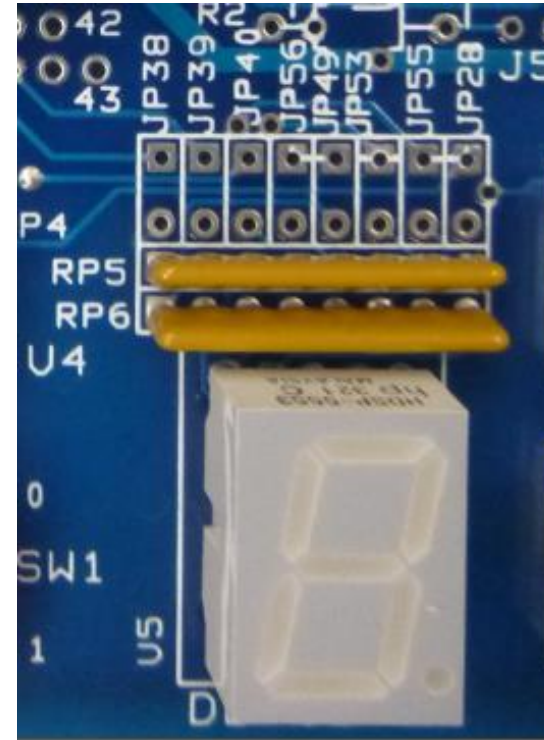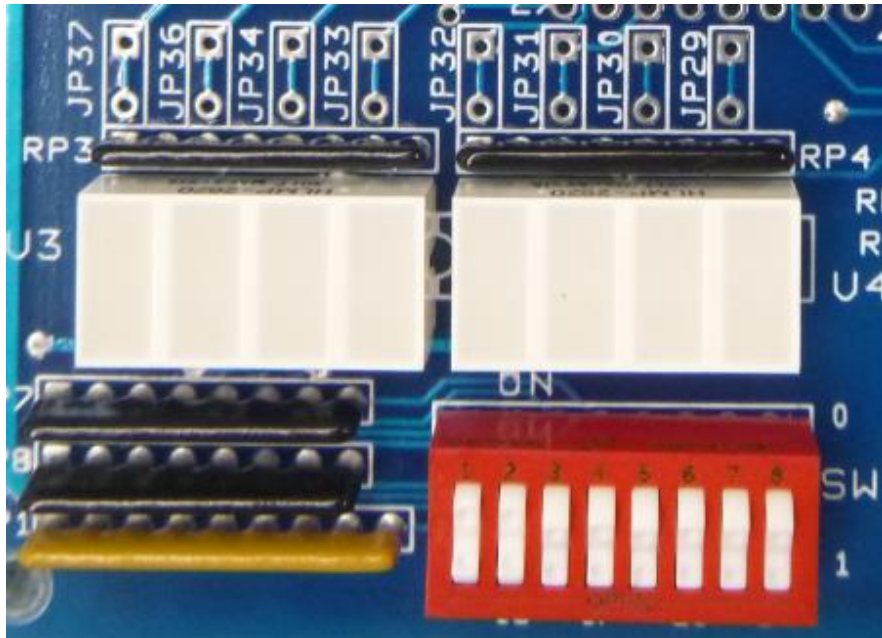
Add Image of Resister Strip

HACK TIME... LETS FIGURE OUT THE BOARD

- Take a look at the board. What do you see?
- Most boards will have a silk screen with cryptic, but possibly useful text
  - What do you see?
  - Can you understand what it's trying to say?
- Hold the board up to the light?
- What can you see?

WHICH PINS ARE CONNECTED TO WHAT?

- Looking at the board, is there any way to determine what "FPGA" pins are connected to the LEDs?

- What About a Data Sheet?

- How could you determine this experimentally?

BOARD PIN OUT

9	7	5	3	1	67	65	63	61
	8	6	4	2	68	66	64	62
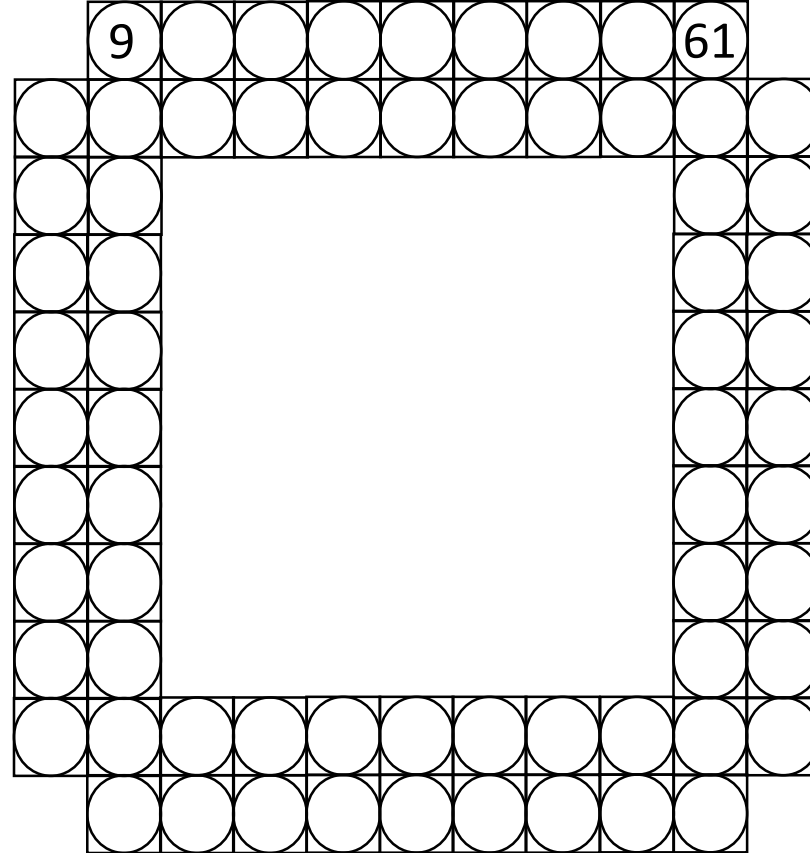
9 ... 61

10	11
12	13
14	15
16	17
18	19
20	21
22	23
24	25
26	

	60
59	58
57	56
55	54
53	52
51	50
49	48
47	46
45	44

28	30	32	34	36	38	40	42
27	29	31	33	35	37	39	41	43

DATA SHEET PIN OUT

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
10	10	PWRDN	12
11	11	TCLKIN-I/O	13
12	—	I/O*	14
13	12	I/O	15
14	13	I/O	16
—	—	I/O	17
15	14	I/O	18
16	15	I/O	19
—	16	I/O	20
17	17	I/O	21
18	18	VCC	22
19	19	I/O	23
—	—	I/O	24
20	20	I/O	25
—	21	I/O	26
21	22	I/O	27
22	—	I/O	28
23	23	I/O	29
24	24	I/O	30
25	25	M1-RDATA	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33
28	28	HDC-I/O	34
29	29	I/O	35
30	30	LDC-I/O	36
—	31	I/O	37
—	—	I/O*	38
31	32	I/O	39
32	33	I/O	40
33	—	I/O*	41
34	34	INIT-I/O	42
35	35	GND	43
36	36	I/O	44
37	37	I/O	45
38	38	I/O	46
39	39	I/O	47
—	40	I/O	48
—	41	I/O	49
40		I/O*	50
41		I/O*	51
42	42	I/O	52
43	43	XTL2(IN)-I/O	53

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	RESET	54
45	45	DONE-PG	55
46	46	D7-I/O	56
47	47	XTL1(OUT)-BCLKIN-I/O	57
48	48	D6-I/O	58
—	—	I/O	59
49	49	D5-I/O	60
50	50	CS0-I/O	61
51	51	D4-I/O	62
—	—	I/O	63
52	52	VCC	64
53	53	D3-I/O	65
54	54	CS1-I/O	66
55	55	D2-I/O	67
—	—	I/O	68
—	—	I/O*	69
56	56	D1-I/O	70
57	57	RDY/BUSY-RCLK-I/O	71
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74
61	61	A0-WS-I/O	75
62	62	A1-CS2-I/O	76
63	63	A2-I/O	77
64	64	A3-I/O	78
—	—	I/O*	79
—	—	I/O*	80
65	65	A15-I/O	81
66	66	A4-I/O	82
67	67	A14-I/O	83
68	68	A5-I/O	84
1	1	GND	1
2	2	A13-I/O	2
3	3	A6-I/O	3
4	4	A12-I/O	4
5	5	A7-I/O	5
—	—	I/O*	6
—	—	I/O*	7
6	6	A11-I/O	8
7	7	A8-I/O	9
8	8	A10-I/O	10
9	9	A9-I/O	11
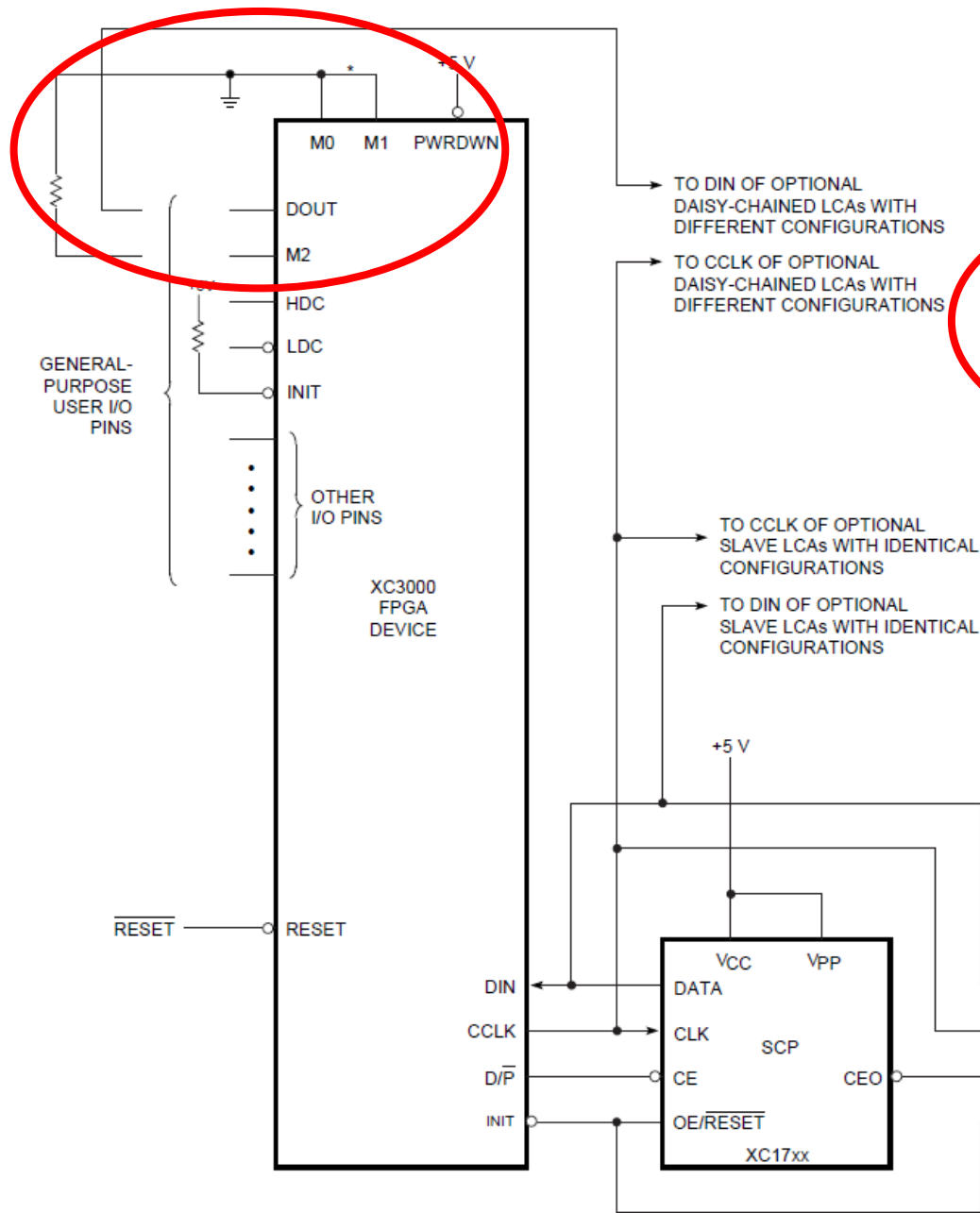
As shown in Table 1, five configuration mode choices are available as determined by the input levels of three mode pins; M0, M1 and M2.

Table 1. Configuration Mode Choices

M0	M1	M2	CCLK	Mode	Data
0	0	0	output	Master	Bit Serial
0	0	1	output	Master	Byte Wide Addr. = 0000 up
0	1	0	—	reserved	—
0	1	1	output	Master	Byte Wide Addr. = FFFF down
1	0	0	—	reserved	—
1	0	1	output	Peripheral	Byte Wide
1	1	0	—	reserved	—
1	1	1	input	Slave	Bit Serial

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
23	23	I/O	29
24	24	I/O	30
25	25	M1-RDATA	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33
28	28	HDC-I/O	34
29	29	I/O	35
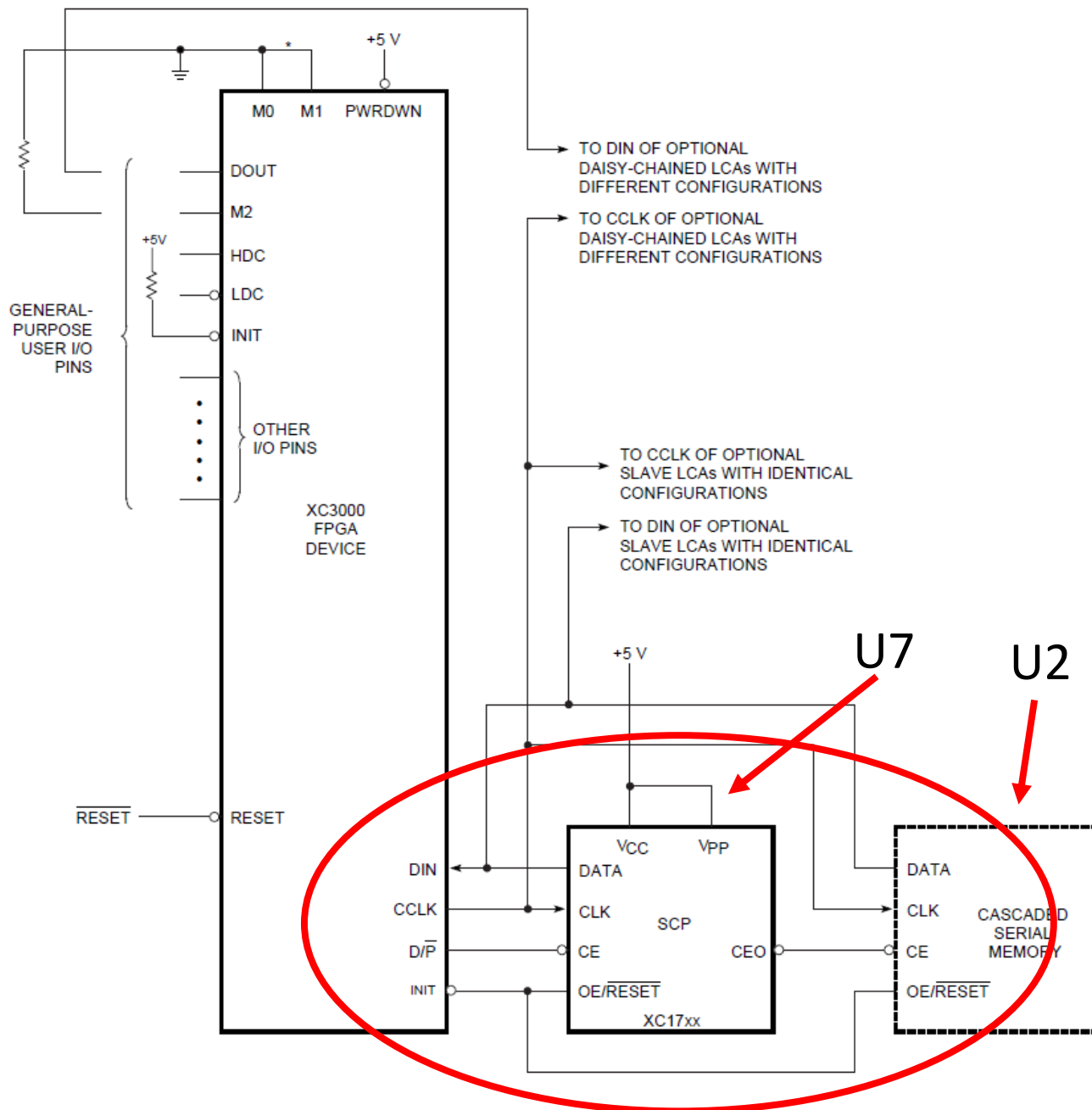
68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
33	—	I/O*	41
34	34	$\overline{\text{INIT}}$-I/O	42
35	35	GND	43

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	$\overline{\text{RESET}}$	54
45	45	DONE-$\overline{\text{PG}}$	55
46	46	D7-I/O	56

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74

Pin	Label	Pin	Label	Pin	Label	Pin	Label
61		10	(PWRDN)	27	(M2)	44	(RESET)
62		11	(TCLKIN / IO)	28	(DP)	45	(DONE)
63		12	SW7	29	LED0	46	
64		13	SW6	30	LED1	47	(XTL1 / BCLK)
65		14		31	LED2	48	
66		15	SW5	32	LED3	49	E
67		16		33	LED4	50	
68		17	SW4	34	LED5	51	
1	GND	18	VCC	35	GND	52	VCC
2		19	SW3	36	LED6	53	F
3		20		37	LED7	54	
4		21	SW2	38	A	55	G
5		22		39	B	56	D
6		23	SW1	40	C	57	
7		24	SW0	41		58	(DIN / IO)
8		25	(M1)	42		59	
9		26	(M0)	43	(XTL2 / IO)	60	(CLK)

UPDATE with Data Sheet Labels

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USING A DMM

- Finding VCC & GND rails
- What else? Could we find the FPGA pin That is connected to the LED 0 Pin?

- Show connector and power pins, and U7 and U2 what are they connected too?
- What about JP29

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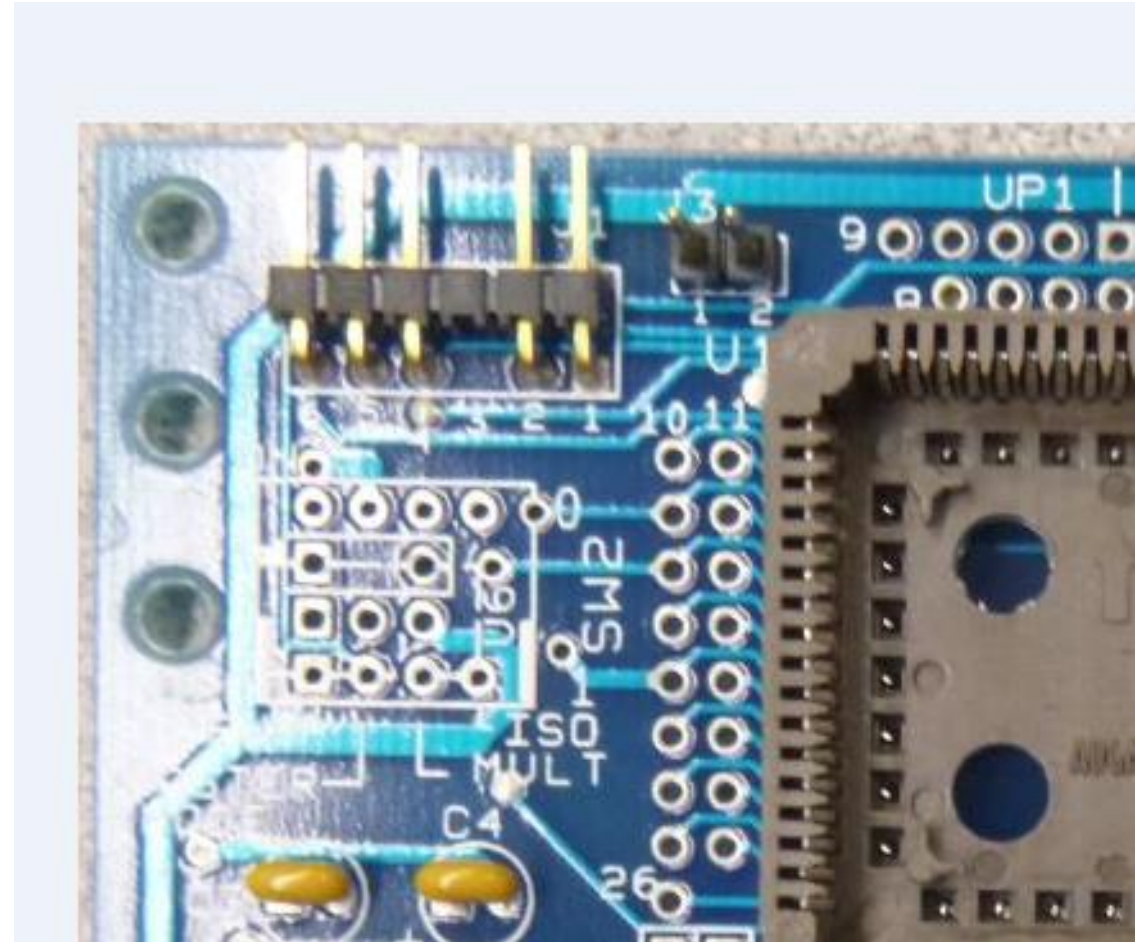&
Squeaky Hinge
PRODUCTIONS

WHY USE A LIMIT OR PULL UP/DOWN RESISTOR?

- Look at the DIP Switches
  - What FPGA pin is DIP Switch 0 connected to?
  - Does it have a pull up or pull down resistor?
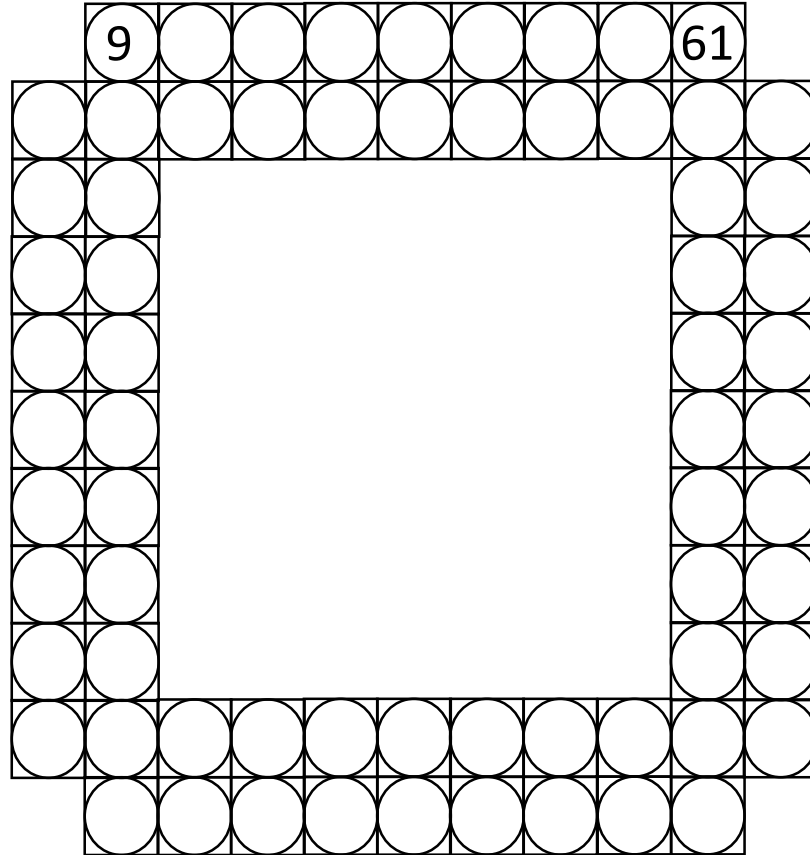 - What is the value?
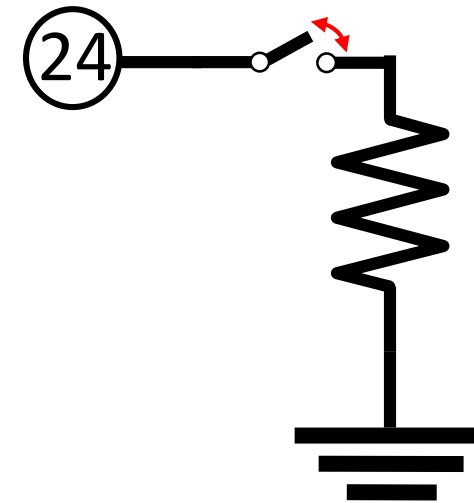
CONNECTING 5 VOLTS?

- This board was meant be powered with 5 volts
- LED and Switches have Pull

PIN OUT

Pin		Pin		Pin		Pin	
61		10	?	27	SW2-2(25)(26)	44	PB-4
62		11	DPSW-1 (MSB)	28	(DP)	45	PB-3 / J1-5
63		12		29	LED0	46	
64		13	DPSW-2	30	LED1	47	?
65		14		31	LED2	48	
66		15	DPS-3	32	LED3	49	E
67		16		33	LED4	50	
68		17	DPSW-4	34	LED5	51	
1	GND	18	VCC	35	GND	52	VCC
2		19	DPSW-5	36	LED6	53	F
3		20		37	LED7	54	
4		21	DPSW-6	38	A	55	G
5		22		39	B	56	D
6		23	DPSW-7	40	C	57	
7		24	DPSW-8 (LSB)	41		58	J1-6/U8-1/U2-1
8		25	SW2-2(26)(27)	42		59	J1-4 / U7-2
9		26	SW2-2(25)(27)	43	?	60	U8-2/U2-2(CLK)

VCC	J2-1 / J3-1 U7-8 / U8-7 U2-8 / U2-7
GND	J2-2 / J3-2 U7-5 U2-5

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OTHER PIN / THROUGH HOLE CONNECTIONS

Show other pin connections, like Proms and jumpers

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POWER?

- Typically you will pull power from Arduino/Pi

- Could hack programing cables to have power and I^2C or other "port"

- Will want to link "VCC" & "GND" from Arduino/Pi
  - Use custom cable connected to J3

APPENDIX

LED Schematic

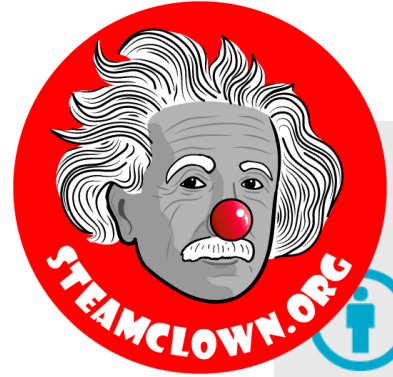# APPENDIX A: LICENSE & ATTRIBUTION

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APPENDIX B: ATTRIBUTION FOR SOURCES USED

- Capture and host Xilinx data sheets and docs

REFERENCE SLIDES

PIN OUT

9	7	5	3	1	67	65	63	61
8	6	4	2	68	66	64	62

10	11
12	13
14	15
16	17
18	19
20	21
22	23
24	25
26

	60
59	58
57	56
55	54
53	52
51	50
49	48
47	46
45	44
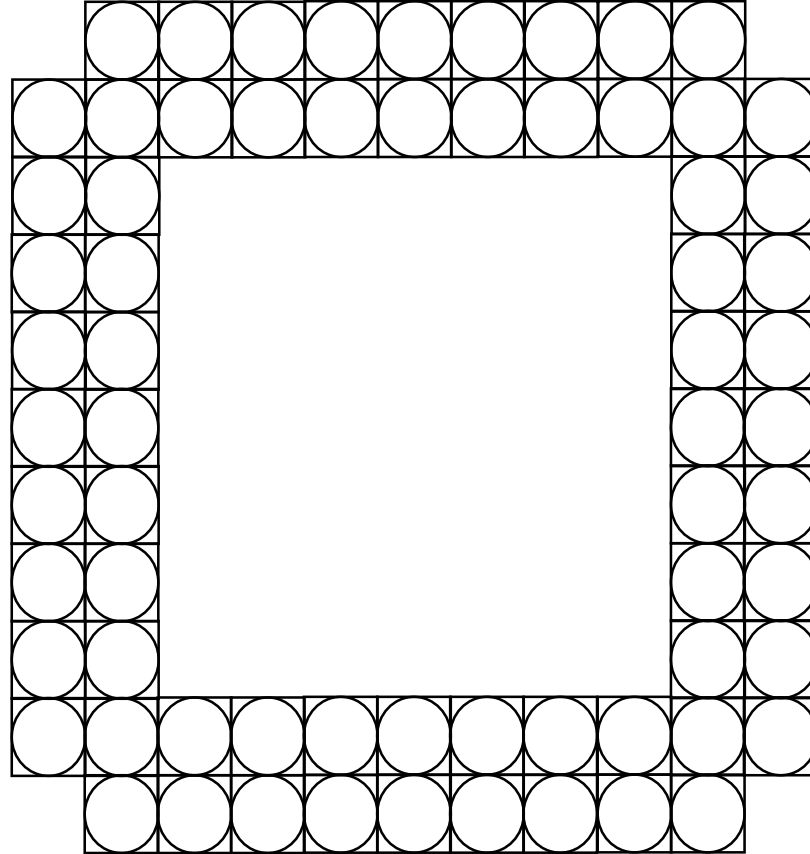
28	30	32	34	36	38	40	42	
27	29	31	33	35	37	39	41	43

CONFIG LOGIC

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
10	10	$\overline{\text{PWRDN}}$	12
11	11	TCLKIN-I/O	13
12	—	I/O*	14
13	12	I/O	15
14	13	I/O	16
—	—	I/O	17
15	14	I/O	18
16	15	I/O	19
—	16	I/O	20
17	17	I/O	21
18	18	VCC	22
19	19	I/O	23
—	—	I/O	24
20	20	I/O	25
—	21	I/O	26
21	22	I/O	27
22	—	I/O	28
23	23	I/O	29
24	24	I/O	30
25	25	M1-$\overline{\text{RDATA}}$	31
26	26	M0-RTRIG	32
27	27	M2-I/O	33

68 PLCC		XC3020A, XC3030A, XC3042A	84 PLCC
XC3030A	XC3020A		
44	44	$\overline{\text{RESET}}$	54
45	45	DONE-$\overline{\text{PG}}$	55
46	46	D7-I/O	56
47	47	XTL1(OUT)-BCLKIN-I/O	57
48	48	D6-I/O	58
—	—	I/O	59
49	49	D5-I/O	60
50	50	$\overline{\text{CS0}}$-I/O	61
51	51	D4-I/O	62
—	—	I/O	63
52	52	VCC	64
53	53	D3-I/O	65
54	54	$\overline{\text{CS1}}$-I/O	66
55	55	D2-I/O	67
—	—	I/O	68
—	—	I/O*	69
56	56	D1-I/O	70
57	57	RDY/BUSY-RCLK-I/O	71
58	58	D0-DIN-I/O	72
59	59	DOUT-I/O	73
60	60	CCLK	74
61	61	A0-$\overline{\text{WS}}$-I/O	75

27	27	M2-I/O	33	61	61	A0-$\overline{\text{WS}}$-I/O	75
28	28	HDC-I/O	34	62	62	A1-CS2-I/O	76
29	29	I/O	35	63	63	A2-I/O	77
30	30	$\overline{\text{LDC}}$-I/O	36	64	64	A3-I/O	78
—	31	I/O	37	—	—	I/O*	79
—		I/O*	38	—	—	I/O*	80
31	32	I/O	39	65	65	A15-I/O	81
32	33	I/O	40	66	66	A4-I/O	82
33	—	I/O*	41	67	67	A14-I/O	83
34	34	$\overline{\text{INIT}}$-I/O	42	68	68	A5-I/O	84
35	35	GND	43	1	1	GND	1
36	36	I/O	44	2	2	A13-I/O	2
37	37	I/O	45	3	3	A6-I/O	3
38	38	I/O	46	4	4	A12-I/O	4
39	39	I/O	47	5	5	A7-I/O	5
—	40	I/O	48	—	—	I/O*	6
—	41	I/O	49	—	—	I/O*	7
40		I/O*	50	6	6	A11-I/O	8
41		I/O*	51	7	7	A8-I/O	9
42	42	I/O	52	8	8	A10-I/O	10
43	43	XTL2(IN)-I/O	53	9	9	A9-I/O	11